REMARKS

This application has been reviewed in light of the Office Action dated September 4, 2002. Claims 1-3 and 7-11 are pending in this application, with Claims 1 and 8 in independent form. Claims 1, 3, 7, and 8 have been amended to define still more clearly what Applicants regard as their invention. Claim 11 has been added to provide Applicants with a more complete scope of protection. Favorable reconsideration is requested.

The Examiner has objected to Figures 1-4 as illustrating only that which is old. Applicants submit herewith, a copy of the Submission of Corrected Drawings filed on April 27, 2001, which labeled Figures 1-5 "PRIOR ART" as required by the Examiner's Amendment mailed January 11, 2001 in the parent application 09/185,717, now U.S. Patent No. 6,245,601. Applicants believe that this submission obviates the objection to the drawings, and its withdrawal is therefore respectfully requested.

The Office Action includes a rejection of Claims 1-3 and 7-10 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,591,963 (Takeda et al.) in view of various combinations of Applicants' disclosure of conventional techniques, U.S. Patent No. 5,591,960 (Furukawa et al.), U.S. Patent No. 4,740,710 (Arita), U.S. Patent No. 5,596,198 (Perez-Mendez), and U.S. Patent No. 4,696,022 (Sashin et al.). Applicants respectfully traverse these rejections.

Applicants submit that independent Claims 1 and 8, together with the remaining dependent claims, are patentably distinct from the proposed combination of the cited prior art at least for the following reasons.

Claim 1 requires a photoelectric converter comprising a photoelectric conversion element of a laminated structure including: a first electrode layer; an insulation layer for blocking the passage of holes and electrons; a photoelectric conversion semiconductor layer; an injection blocking layer for blocking the injection of only one of the holes or the electrons to the photoelectric conversion semiconductor layer at a time; a second electrode layer; and a switching means for operating the photoelectric converter by switching through the following three operation modes: (a) an idling mode for emitting one of the holes or the electrons from the photoelectric conversion element; (b) a photoelectric conversion mode for accumulating one of the holes or the electrons generated in accordance with an amount of incident light; and (c) a refresh mode for emitting the holes or the electrons accumulated in the photoelectric conversion element.

One important feature of Claim 1 is the insulation layer for blocking the passage of holes and electrons, the injection blocking layer for blocking the injection of only one of the holes and electrons to the photoelectric conversion semiconductor layer at a time, and the switching means for operating the photoelectric converter in an idling mode. This feature is described in the specification at least at page 16, line 17 to page 17, line 8 in reference to Figure 6A, which states in part that:

> "[r]eference numeral 70 denotes an insulation layer formed of silicon nitride (SiN), which blocks the passage of both electrons and holes . . . [and reference] numeral 5 denotes an injection blocking layer formed of an n^+ layer of a-Si to block the injection of holes from the side of a transparent electrode 6 to the photoelectric conversion semiconductor layer 4."

Further support for this feature can be found in the specification at least at page 47, line 10 to page 48, line 16 in reference to Figure 19. This portion of the specification states in part that "$0 < V_{dg}[idle] < V_{dg}[read]$." In other words, the voltage difference in the idle mode is greater than 0V, but less than the positive voltage applied in a photoelectric conversion (read) mode. Note that electrode "D" and electrode "G" in Figure 19 correspond to the transparent electrode 6 and the lower electrode 2 respectively, in Figures 6A and 17A. (It is to be understood, of course, that the scope of Claim 1 is not limited to the details of this embodiment, which is referred to only for purposes of illustration.)

Takeda et al. relates to a photoelectric conversion device with dual insulating layers. Takeda et al. discloses lower and upper insulating layers 70 and 71 in Figures 4A and 11A, and at column 7, lines 26-42, as referred to by the Examiner. (See pages 3 and 4 of the Office Action). Applicants' discussion of the prior art discloses a p-type semiconductor layer 3 and an n-type semiconductor layer 5 in reference to Figure 1. Neither of which are insulating layers. (See page 2 of the specification). The Examiner states that Takeda et al does "not necessarily teach the further limitation that the layer 71 should block either holes or electrons only. However, as admitted prior art Applicant describes . . . a photoelectric converter in which at the position of insulating layer 71 as

taught by Takeda et al there is instead a semiconductor layer of second conductivity type, hence capable of selectively blocking the charge carriers of first conductivity type . . . ." (Page 4 of the Office Action). Applicants understand the Examiner's position to be that swapping insulation layer 71 in Takeda et al. with an n-type semiconductor layer 5 discussed in Applicants' specification would be obvious. Applicants respectfully traverse this position.

In particular, to swap insulation layer 71 in Takeda et al. with an n-type semiconductor layer 5 would lead to a photoelectric conversion device with both an insulation layer and an injection blocking layer, as recited in Claim 1 of the present invention. But, Takeda et al. specifically teaches away from such a scenario. Takeda et al. at column 6, lines 48-53 states that "[t]he present invention has been achieved . . . to provide a photoelectric conversion device capable of detecting the amount of incident light *without providing an injection blocking layer* within the photoelectric conversion device . . ." (emphasis added). Therefore, a person having ordinary skill in the art reading Takeda et al. would specifically *not* look to have both an injection blocking layer and an insulating layer in the same photoelectric conversion device, as recited in Claim 1.

With regard to the idling mode, the Examiner states that in Example 2, Fig. 9 of Takeda et al., "there is no explicit mention of an idling mode, [but that] it is obvious from Fig. 4B and the discussion of Example 1 . . . ." (Page 5 of the Office Action). The Examiner goes on to state that "the essence of the idling mode (recess mode in Applicant's disclosure) in other embodiments of the invention by Takeda et al is present . . . for the

obvious purpose to have the option of setting $V_{UB} = 0 \ldots$." Applicants also respectfully traverse this position.

The idling mode of the present invention is not equivalent to the recess mode in Applicants' disclosure. The recess mode of Applicants' disclosure refers to a "stop" mode where both ends of the photoelectric conversion element are set to the same potential, GND. (See page 18, lines 4-12 of the specification). In other words, the recess mode is characterized by $V_{dg} = 0$, where V_{dg} corresponds with V_{UB} in Takeda et al. In contrast, the idling mode allows for the emitting of one of the holes or the electrons from the photoelectric conversion element, as recited in Claim 1, by having a voltage V_{dg} which is *greater* than zero, but smaller than the positive voltage V_{dg} which exists in the photoelectric conversion (read) mode. In other words, the idling mode requires a potential difference V_{dg} obtained by subtracting the potential of the second electrode layer from the potential of the first electrode layer of the photoelectric conversion element in the idling mode to be smaller than a potential difference V_{dg} obtained by subtracting the potential of the second electrode layer from the potential of the first electrode layer of the photoelectric conversion element in the photoelectric conversion mode, as recited in dependent Claim 2. Takeda et al. and Applicants' disclosure are both silent to such a feature, as evidenced in part by Figure 4B in Takeda et al. which discloses only a read and refresh mode.

Applicants submit that, at least for the reasons discussed above, the proposed combination of Takeda et al. and Applicants' disclosure, assuming such combination would even be permissible, would still fail to teach or suggest the insulation

layer for blocking the passage of holes and electrons, the injection blocking layer for blocking the injection of only one of the holes and electrons to the photoelectric conversion semiconductor layer at a time, and the switching means for operating the photoelectric converter in an idling mode, as recited in independent Claim 1. Accordingly, Applicants submit that Claim 1 is patentable over these references, taken separately or in any proper combination.

Independent Claim 8 includes the same feature of the insulation layer for blocking the passage of holes and electrons, the injection blocking layer for blocking the injection of only one of the holes and electrons to the photoelectric conversion semiconductor layer at a time, and the switching means for operating the photoelectric converter in an idling mode, as discussed above in connection with Claim 1. Applicants have reviewed the additional references Perez-Mendez and Sashin et al. used to reject Claim 8, and have failed to find anything that, in Applicants' opinion, would remedy the deficiencies of the art discussed above, as applied against independent Claim 1. Accordingly, Claim 8 is believed to be patentable for at least the same reasons as discussed above in connection with Claim 1.

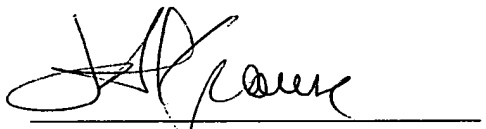
A review of the other art of record has failed to reveal anything that, in Applicants' opinion, would remedy the deficiencies of the art discussed above, as applied against the independent claims herein. Therefore, those claims are respectfully submitted to be patentable over the art of record.

The other rejected claims in this application depend from one or another of the independent claims discussed above, and, therefore, are submitted to be patentable for at least the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, individual consideration or reconsideration, as the case may be, of the patentability of each claim on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration and early passage to issue of the present application.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE TO CLAIMS

1. (Thrice Amended) A photoelectric converter comprising a photoelectric conversion element of a laminated structure comprising:

a first electrode layer;

an insulation layer for blocking the passage of holes and electrons;

a photoelectric conversion semiconductor layer;

an injection blocking layer for blocking the injection of only one of the holes [and] or the electrons to the photoelectric conversion semiconductor layer at a time;

a second electrode layer; and

a switching means for operating the photoelectric converter by switching through the following three operation modes a) through c):

a) an idling mode for emitting one of the holes or the electrons from the photoelectric conversion element;

[b) a refresh mode for refreshing the other of the holes or the electrons accumulated in the photoelectric conversion element; and]

[c)] b) a photoelectric conversion mode for accumulating [at least] one of [pair of] the holes [and] or the electrons generated in accordance with an amount of incident light; and

c) a refresh mode for emitting the holes or the electrons accumulated in the photoelectric conversion element.

3. (Twice Amended) The photoelectric converter according to claim 1, wherein a recess mode of the photoelectric conversion element is provided for by applying a zero electric field to each layer before the idling mode.

7. (Amended) The photoelectric converter according to claim 1, wherein:

a plurality of the photoelectric conversion elements are arranged one-dimensionally or two-dimensionally,

a switching element is connected for each of the photoelectric conversion elements,

all the photoelectric conversion elements are divided into a plurality of n [blocs] blocks,

a light signal [of n x m of all] from the photoelectric conversion elements divided into n [blocs] blocks is output with a matrix signal wiring by operating the switching element for each of the [blocs] blocks,

an intersection part of the matrix signal wiring comprises a lamination structure in which at least a first electrode layer, an insulating layer, a semiconductor layer and a second electrode layer are provided in this order, [and] each [layer of the lamination structure is formed with the same layer as each of] corresponding to the first electrode layer, the insulating layer, the photoelectric conversion semiconductor layer, and the second electrode layer of the photoelectric conversion element.

8. (Thrice Amended) A system comprising:

a photoelectric converter comprising a photoelectric conversion element of a laminated structure comprising:

a first electrode layer;

an insulation layer for blocking the passage of holes and electrons;

a photoelectric conversion semiconductor layer;

an injection blocking layer for blocking the injection of only one of the holes [and] or the electrons to the photoelectric conversion semiconductor layer at a time;

a second electrode layer; and

a switching means is provided for operating the photoelectric converter by switching through the following three operation modes a) through c):

a) an idling mode for emitting one of the holes or the electrons from the photoelectric conversion element;

[b) a refresh mode for refreshing the other of the holes or the electrons accumulated in the photoelectric conversion element; and]

[c)] b) a photoelectric conversion mode for accumulating [at least] one of [pair of] the holes [and] or the electrons generated in accordance with an amount of incident light; and

c) a refresh mode for emitting the holes or the electrons accumulated in the photoelectric conversion element;

a signal processing means for processing a signal from the photoelectric converter;

a recording means for recording a signal from the signal processing means;

a display means for displaying a signal from the signal processing means;

an electric transmission means for electrically transmitting a signal from the signal processing means; and

a radiation source for generating radiation.